What is claimed is:

1. A method of fabricating field effect transistors having low sheet resistance gate electrodes, comprising the steps of:

providing a semiconductor substrate, said substrate having been provided with at least one gate electrode created over an active surface region as said substrate as defined by regions of Shallow Trench Isolation provided in the surface of the said substrate, said at least one gate electrode having been provided with gate spacers, impurity implants of source and drain regions in addition to Lightly Doper Diffusion regions having been provided in the surface of said substrate self-aligned with said at least one gate electrode, said at least one gate electrode comprising a layer of pad oxide created over the surface of said substrate over which a layer of polysilicon has been patterned;

depositing a thin layer of salicide material over the surface of said substrate, including the surface of said gate spacers and said layer of polysilicon provided for said at least one gate electrode;

performing a first anneal, creating reacted and unreacted salicide material, forming salicided layers comprising said reacted salicide material over the surface of said source and drain implants;

first removing said unreacted salicide material from the surface of said substrate;

depositing a layer of etch stop material over the surface of said substrate, including the surface of said gate spacers and said layer of polysilicon provided for said at least one gate electrode;

depositing a layer of dielectric over the surface of said layer of etch stop material to an adequate thickness such that the surface of said layer of dielectric extends above the surface of said layer of etch stop material even where said etch stop material overlays the surface of said at least one gate electrode;

polishing the surface of said layer of dielectric down to the surface of said layer of etch stop material where said layer of etch stop material overlays the surface of said at least one gate electrode, using said layer of etch stop material as a stop for said process of polishing;

removing said layer of etch stop material from above said at least one gate electrode, exposing the surface of said layer of polysilicon forming part of said at least one gate electrode;

depositing a thick layer of salicide material over the surface of said polished layer of dielectric, including the exposed surface of said layer of polysilicon;

performing a second anneal of said deposited thick layer of salicide material, creating reacted and unreacted salicide

material, a layer of reacted salicide material overlying said layer of polysilicon of said at least one gate electrode;

second removing unreacted salicide material from the surface of said layer of dielectric;

performing a third anneal, reducing the sheet resistance of said reacted salicide material overlying said layer of polysilicon of said at least one gate electrode.

2. The method of claim 1 wherein said depositing a thin layer of salicide material over the surface of said substrate comprises depositing a thin layer of Ti/TiN, deposited to a thickness between about 100 and 500 Angstrom and more preferably to a thickness of about 300 Angstrom.

3. The method of claim 1 wherein said first anneal is a low temperature anneal performed by rapid thermal annealing in a temperature range of between about 600 and 850 degrees C. for a time between about 20 and 60 seconds.

4. The method of claim 1 wherein said first removing said unreacted salicide material from the surface of said substrate comprises performing a selective wet etch.

5. The method of claim 1 wherein said depositing a layer of etch stop material over the surface of said substrate comprises depositing a layer of silicon nitride.

6. The method of claim 1 wherein said depositing a layer of dielectric over the surface of said layer of etch stop material comprises depositing a layer of boro-phosphate-silicate-glass (BPSG).

7. The method of claim 1 wherein said removing said layer of etch stop material from above said at least one gate electrode comprises applying an Reactive Ion Etch.

8. The method of claim 1 wherein said depositing a thick layer of salicide material over the surface of said polished layer of dielectric comprises depositing a layer of Ti/TiN, deposited to a thickness between about 2,000 to 5,000 Angstrom.

9. The method of claim 1 wherein said performing a second anneal of said deposited thick layer of salicide material comprises performing a low temperature anneal performed by rapid thermal annealing in a temperature range of between about 600 and 850 degrees C. for a time between about 20 and 60 seconds.

10. The method of claim 1 wherein said second removing unreacted salicide material from the surface of said layer of dielectric comprises performing a selective wet etch.

11. The method of claim 1 wherein said third anneal comprises rapid thermal annealing in a temperature range of between about 850 and 1000 degrees C. for a time between about 20 and 60 seconds.

12. A method of fabricating field effect transistors having low sheet resistance gate electrodes, comprising the steps of:

providing a semiconductor substrate, said substrate having been provided with at least one gate electrode created over an active surface region as said substrate as defined by regions of Shallow Trench Isolation provided in the surface of the said substrate, said at least one gate electrode having been provided with gate spacers, impurity implants of source and drain regions in addition to Lightly Doper Diffusion regions having been provided in the surface of said substrate self-aligned with said at least one gate electrode, said at least one gate electrode comprising a layer of pad oxide created over the surface of said substrate over which a layer of polysilicon has been patterned;

depositing a thin layer of Ti/TiN over the surface of said substrate, including the surface of said gate spacers and said

layer of polysilicon provided for said at least one gate electrode, deposited to a thickness between about 100 and 500 Angstrom and more preferably to a thickness of about 300 Angstrom;

performing a low temperature anneal of said deposited thin layer of Ti/TiN in a temperature range of between about 600 and 850 degrees C. for a time between about 20 and 60 seconds, creating a layer of $TiSi_x$ over the surface of said source and drain implants, leaving uncreated Ti/TiN in place over the surface of said Shallow Trench Isolation regions;

removing said uncreated Ti/TiN from the surface of said substrate by performing a selective wet etch;

depositing a layer of silicon nitride over the surface of said substrate, including the surface of said gate spacers and said layer of polysilicon provided for said at least one gate electrode;

depositing a layer of boro-phosphate-silicate-glass (BPSG) over the surface of said layer of silicon nitride to an adequate thickness such that the surface of said layer of boro-phosphate-silicate-glass (BPSG) extends above the surface of said layer of silicon nitride even where said silicon nitride overlays the surface of said at least one gate electrode;

polishing the surface of said layer of boro-phosphate-silicate-glass (BPSG) down to the surface of said layer of

silicon nitride where said layer of silicon nitride overlays the surface of said at least one gate electrode, using said layer of silicon nitride as a stop for said process of polishing;

removing said layer of silicon nitride from above said at least one gate electrode by applying an Reactive Ion Etch, exposing the surface of said layer of polysilicon forming part of said at least one gate electrode;

depositing a thick layer of Ti/TiN over the surface of said polished layer of boro-phosphate-silicate-glass (BPSG), including the exposed surface of said layer of polysilicon, deposited to a thickness between about 2,000 to 5,000 Angstrom ;

performing an anneal of said deposited thick layer of Ti/TiN by rapid thermal annealing in a temperature range of between about 600 and 850 degrees C. for a time between about 20 and 60 seconds, creating a layer of $TiSi_x$ overlying said layer of polysilicon of said at least one gate electrode;

removing unreacted Ti/TiN from the surface of said layer of BPSG by performing a selective wet etch; and

performing an anneal of said layer of $TiSi_x$, comprising a rapid thermal annealing in a temperature range of between about 850 and 1000 degrees C. for a time between about 20 and 60 seconds, reducing the sheet resistance of said reacted salicide material overlying said layer of polysilicon of said at least one gate electrode.

13. A method of fabricating field effect transistors having low sheet resistance gate electrodes, comprising the steps of:

providing a semiconductor substrate, said substrate having been provided with at least one gate electrode created over an active surface region as said substrate as defined by regions of Shallow Trench Isolation provided in the surface of the said substrate, said at least one gate electrode having been provided with gate spacers, impurity implants of source and drain regions in addition to Lightly Doper Diffusion regions having been provided in the surface of said substrate self-aligned with said at least one gate electrode, said at least one gate electrode comprising a stack of layers of pad oxide created over the surface of said substrate, a layer of polysilicon patterned over the layer of pad oxide and a layer of boronitride patterned over the layer of polysilicon;

depositing a thin layer of salicide material over the surface of said substrate, including the surface of said gate spacers and said layer of polysilicon provided for said at least one gate electrode;

performing a first anneal, creating reacted and unreacted salicide material, forming salicided layers comprising said reacted salicide material over the surface of said source and drain implants;

first removing said unreacted salicide material from the surface of said substrate;

depositing an isolation film over the surface of said substrate, including the surface of said gate spacers and said layer of boronitride provided for said at least one gate electrode;

depositing a layer of filler material over the surface of said isolation film to an adequate thickness such that the surface of said layer of filler material extends above the surface of said isolation film even where said isolation film overlays the surface of said at least one gate electrode;

polishing the surface of said layer of filler material and said layer of isolation film down to the surface of said layer of boronitride of said at least one gate electrode, using said layer of boronitride as a stop for said process of polishing;

removing said layer of boronitride from said at least one gate electrode, exposing the surface of said layer of polysilicon forming part of said at least one gate electrode;

depositing a thick layer of salicide material over the surface of said polished layer of filler material, including the exposed surface of said layer of polysilicon;

performing a second anneal of said deposited thick layer of salicide material, creating reacted and unreacted salicide

material, a layer of reacted salicide material overlying said layer of polysilicon of said at least one gate electrode;

second removing unreacted salicide material from the surface of said layer of dielectric;

performing a third anneal, reducing the sheet resistance of said reacted salicide material overlying said layer of polysilicon of said at least one gate electrode.

14. The method of claim 13 wherein said depositing a thin layer of salicide material over the surface of said substrate comprises depositing a thin layer of Ti/TiN, deposited to a thickness between about 100 and 500 Angstrom and more preferably to a thickness of about 300 Angstrom.

15. The method of claim 13 wherein said first anneal is a low temperature anneal performed by rapid thermal annealing in a temperature range of between about 600 and 850 degrees C. for a time between about 20 and 60 seconds.

16. The method of claim 13 wherein said first removing said unreacted salicide material from the surface of said substrate comprises performing a selective wet etch.

17. The method of claim 13 wherein said depositing an isolation film over the surface of said substrate comprises depositing a layer of silicon oxide.

18. The method of claim 13 wherein said depositing a layer of filler material over the surface of said layer of etch stop material comprises depositing a layer of photoresist.

19. The method of claim 13 wherein said removing said layer of boronitride from said at least one gate electrode comprises applying a Reactive Ion Etch.

20. The method of claim 13 wherein said depositing a thick layer of salicide material over the surface of said polished layer of filler material comprises depositing a layer of Ti/TiN, deposited to a thickness between about 2,000 to 5,000 Angstrom.

21. The method of claim 13 wherein said performing a second anneal comprises performing a low temperature anneal performed by rapid thermal annealing in a temperature range of between about 600 and 850 degrees C. for a time between about 20 and 60 seconds.

22. The method of claim 13 wherein said second removing unreacted salicide material from the surface of said layer of filler material comprises performing a selective wet etch.

23. The method of claim 13 wherein said third anneal comprises rapid thermal annealing in a temperature range of between about 850 and 1000 degrees C. for a time between about 20 and 60 seconds.

24. A method of fabricating field effect transistors having low sheet resistance gate electrodes, comprising the steps of:

providing a semiconductor substrate, said substrate having been provided with at least one gate electrode created over an active surface region as said substrate as defined by regions of Shallow Trench Isolation provided in the surface of the said substrate, said at least one gate electrode having been provided with gate spacers, impurity implants of source and drain regions in addition to Lightly Doper Diffusion regions having been provided in the surface of said substrate self-aligned with said at least one gate electrode, said at least one gate electrode comprising a stack of layers of pad oxide created over the surface of said substrate, a layer of polysilicon patterned over the layer of pad oxide and a layer of boronitride patterned over the layer of polysilicon;

depositing a thin layer of Ti/TiN over the surface of said substrate, including the surface of said gate spacers and said layer of polysilicon provided for said at least one gate electrode, deposited to a thickness between about 100 and 500 Angstrom and more preferably to a thickness of about 300 Angstrom;

performing a low temperature anneal of said deposited thin layer of Ti/TiN in a temperature range of between about 600 and 850 degrees C. for a time between about 20 and 60 seconds, creating a layer of $TiSi_x$ over the surface of said source and drain implants, leaving uncreated Ti/TiN in place over the surface of said Shallow Trench Isolation regions;

removing said uncreated Ti/TiN from the surface of said substrate by performing a selective wet etch;

depositing a layer of silicon oxide over the surface of said substrate, including the surface of said gate spacers and said layer of boronitride provided for said at least one gate electrode;

depositing a layer of photoresist over the surface of said layer of silicon oxide to an adequate thickness such that the surface of said layer of photoresist extends above the surface of said layer of silicon oxide even where said silicon oxide overlays the surface of said at least one gate electrode;

polishing the surface of said layer photoresist and said layer of silicon oxide down to the surface of said layer of boronitride being part of at least one gate electrode, using said layer of boronitride as a stop for said process of polishing;

removing said layer of boronitride from said at least one gate electrode by applying an Reactive Ion Etch, exposing the surface of said layer of polysilicon forming part of said at least one gate electrode;

depositing a thick layer of Ti/TiN over the surface of said polished layer of photoresist, including the exposed surface of said layer of polysilicon, deposited to a thickness between about 2,000 to 5,000 Angstrom ;

performing an anneal of said deposited thick layer of Ti/TiN by rapid thermal annealing in a temperature range of between about 600 and 850 degrees C. for a time between about 20 and 60 seconds, creating a layer of $TiSi_x$ overlying said layer of polysilicon of said at least one gate electrode;

removing unreacted Ti/TiN from the surface of said layer of photoresist by performing a selective wet etch;

performing an anneal of said layer of $TiSi_x$ overlying said layer of polysilicon of said at least one gate electrode, comprising a rapid thermal annealing in a temperature range of between about 850 and 1000 degrees C. for a time between about 20 and 60 seconds, reducing the sheet resistance of said reacted

salicide material overlying said layer of polysilicon of said at least one gate electrode.